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TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

Mark V. Pierson, et al.

For: **FLOATING INTERPOSER**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EJ563657300US**
- ☒ **2** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☒ Information Disclosure Statement
- ☐ Preliminary Amendment
- ☐ Other:

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	22	- 20 =	2	x	$18.00	$36.00
Indep. Claims	4	- 3 =	1	x	$78.00	$78.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$690.00
					TOTAL FILING FEE	$804.00

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Dated: May 24, 2000

Lawrence R. Fraley
Signature

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APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAME:	**MARK V. PIERSON, ET AL.**
TITLE:	**FLOATING INTERPOSER**
DOCKET NO.	**EN9-99-102**

INTERNATIONAL BUSINESS MACHINES CORPORATION

CERTIFICATE OF MAILING UNDER 37 CFR 1.10

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FLOATING INTERPOSER

Background of the Invention

1. Field of the Invention

The present invention relates to an electrical interconnection arrangement for making connection between electronic devices and, more particularly, to making electrical connection between chip die and the next level of carrier.

2. Background and Related Art

One of the problems encountered with some semiconductor chip die connections to the next level of packaging is the high stress on the interconnections caused by coefficient of thermal expansion (CTE) mismatch. The CTE thermal mismatch is particularly large where the chip die is connected to laminate chip carriers made of material similar to an epoxy circuit board material. As circuit densities in chip dies increase, so does the heat generated by these dies thereby compounding the problem with larger temperature variations in its thermal cycle. In addition, certain applications, such as flip chip applications, have required encapsulation to ensure a reliable flip chip interconnection in the solder joints. Such encapsulation typically employs a high strength epoxy which acts to bond the chip die to the laminate

chip carrier. This bonding of chip die to chip carrier reduces solder joint stress during thermal cycling but causes the chip die itself to be put under cyclical high internal stress eventually leading to chip cracking, delamination and device breakdown.

The above described high internal stresses on the chip die are generally attributed to the fact that the bonding of chip die to laminate chip carrier acts to cause this composite of materials to act like a "bimetallic" element wherein the composite bends upon heating due to the different CTE of the materials. As a result of the large thermal mismatch between the die and laminate chip carrier, the cyclical bending over time causes device failure. In this regard, the CTE for a typical chip die may be in the order of 3 micro inches per inch per degree Centigrade while a typical laminate chip carrier is around six times that amount. Thus, although the use of encapsulation is to prevent the C-4 connections from detaching from fatigue and fracturing over thermal cycling, the bonding action of the encapsulation in itself acts to cause the chips to fracture and separate from the chip carrier.

In general, others have attempted to address the problems caused by CTE mismatch of materials in IC packaging by providing various interposing structures that attempt to reduce the mismatch of CTE. For example, multiple layers of materials with varying CTEs may be employed to form an interposing layer between one level of packaging and the next, with the layers having a gradation of CTEs such that the layer contacting one level of packaging is selected to have a CTE which more closely matches the CTE of that level while the layer contacting the next level of packaging has a CTE more closely matching that level while layers between may gradually reduce the difference.

In addition, efforts have also been made to use interposing layers which are flexible in nature such as to reduce the stress on electrical interconnections during thermal cycling created by thermal mismatch. However, these various efforts typically rely on single or multiple layers of material which are either costly to fabricate or difficult to assemble, and are not totally effective in their purpose. More often, these layers are between ceramic chip carriers and circuit board or card.

Summary of the Invention

In accordance with the teachings of the present invention, internal stresses in chip dies and their electrical interconnection caused by encapsulation and bonding of chip dies to laminate chip carriers are overcome through the use of a floating interposer having an array of connectors extending therethrough and positioned between chip die contacts and circuit card contacts. The floating interposer acts as chip carrier and provides stress relief to the electrical interconnections between chip die and circuit card by moving on its opposing surfaces relative to the CTE rate of the material with which it is in contact.

The floating interposer of the present invention comprises a flexible and compliant layer of low modulus material having an array of vias plated with copper which vias terminate in copper pads at each end on opposing surfaces of the flexible layer. In addition, the flexible layer may have an array of relatively large holes arranged between the array of vias to produce a "swiss-cheese-like" structure to give more resilience.

In one fabrication process, when the plated vias of the interposer are aligned with C-4 solder balls on a flip chip die, upon heating the vias become filled with solder while becoming electrically connected to the chip die. The other ends of the vias are attached to the circuit card by a low melt solder. Alternatively, the flexible interposer may be copper plated directly against the BLM pads on the chip die.

Accordingly, it is an object of the present invention to provide an improved integrated circuit device package and method of making same.

It is another object of the present invention to provide improved electronic device interconnection and method of making same.

It is a further object of the present invention to provide improved electronic interconnection between chip die device and chip carrier.

It is yet a further object of the present invention to provide an improved electronic interconnection between chip die and chip carrier such as to reduce internal stress in both the chip die and the electrical interconnections between chip die and chip carrier.

It is still yet a further object of the present invention to provide a flexible interposer arrangement between chip die and chip carrier which allows the chip die to be connected to the chip carrier without encapsulation of the interconnection points.

It is another object of the present invention to provide a method and apparatus for making electrical interconnection between chip die directly to circuit card.

It is yet another object of the present invention to provide a compact, reworkable die solution.

These foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention, as illustrated in the accompanying drawings, wherein like reference members represent like parts of the invention.

Brief Description of the Drawing

Figure 1 shows a partial cross-section of one embodiment of the floating interposer structure of the present invention.

Figure 2 shows a partial top view of a further refinement of the floating interposer of the present invention.

Figure 3 shows a partial cross-section of another embodiment of the floating interposer structure of the present invention.

Figure 4 shows a partial cross-section of yet a further embodiment of the floating interposer structure of the present invention.

Figure 5 shows a partial cross-sectional view of one method and structure for connecting the floating interposer of the present invention to a chip die.

Figure 6 shows a partial cross-sectional view of another method and structure for connecting the floating interposer of the present invention to a chip die.

Figure 7 shows a partial cross-sectional view of a further method and structure for connecting the floating interposer of the present invention to a chip die.

Figure 8 shows a partial cross-sectional view of a method and structure for further connecting the interposer arrangement of Figure 5 to a circuit card.

Figure 9 shows a partial cross-sectional view of a method and structure for further connecting the interposer arrangement of Figure 6 to a circuit card.

Figure 10 shows a partial cross-sectional view of a method and structure for further connecting the interposer arrangement of Figure 7 to a circuit card.

Detailed Description

With reference to Figure 1, there is shown an interposer arrangement, in partial cross-section, fabricated in accordance with the present invention. Interposer 1 is fabricated from a flexible dielectric layer 3 of low modulus material such as, for example, Rogers 2800 material, Dow 1-4173 material or GE 3281 material. Layer 3 may have an elastic modulus in the range of about 50,000 psi to about 400,000 psi. The thickness of flexible dielectric layer 3 may range between 10 to 15 mils. This may be obtained by laminating several layers of Rogers 2800 material, for example, with heat and pressure to form this thickness. An array of vias 5 are formed in the layer, each approximately 2 mils in diameter. These vias may be fabricated by laser ablation, for example. The array of vias are patterned to match the pattern of connection points on the flip chip die and corresponding connection points on the circuit card chip carrier to which it will be interposed and connected. The vias are then copper plated to form copper walls 6. This may be achieved by first plating all of layer 3 with electroless copper. A plating resist is then applied to the vias and both sides of the layer. A mask is aligned to retain resist in the vias and at sites surrounding the end of the vias so as to form top pads 7 and

bottom pad 9 at the respective ends of the copper walls. Each pad may be approximately 4 mils in diameter. The resist is then exposed and developed and exposed copper on both sides removed after which the resist is stripped off. Further plaiting may then be carried out. For some applications, the copper plated vias could then be filled with a conductive adhesive composition, if necessary, but the arrangements shown in Figures 5 and 7 use a different approach.

It should be understood that although in the various embodiments described herein, reference is made to use of copper to form the walls and pads, it is clear that other metals, such as gold or nickel, may also be used in place of copper for plating the various vias and pads. The process for applying these metals is the same as that used for applying copper.

To further reduce stiffness in flexible dielectric layer 1 of Figure 1 and make it more soft and spongy, additional holes 11 may be formed through the layer between the vias to form a "swiss-cheese-like" structure, as shown in Figure 2. These holes may be 3 to 4 mils in diameter and may also be formed by laser ablation. As shown in Figure 2, holes 11 are patterned in an array that compliments the array of vias 5, each hole being approximately equidistant the vias which surround it.

Figure 3 shows a further interposer arrangement in accordance with the present invention. As can be seen, the difference between Figures 1 and 3 is that Figure 3 shows angled or sloped vias 13 with copper plated walls 15 in flexible dielectric layer 3. These vias may also be made by laser ablation and plated as described with respect to Figure 1. The advantage of the sloped plated vias is that this configuration provides additional freedom to flex both

vertically and horizontally. Additional holes, as shown at 11 in Figure 2, may also be fabricated between the vias in the flexible dielectric layer 3 of Figure 3 at the same slope as these vias.

Figure 4 shows yet a further interposer arrangement, in partial cross-section, in accordance with the present invention. As shown in Figure 4, copper plated vias 17 are formed in a V-shape configuration in flexible dielectric layer 3. Again, the configuration allows for additional freedom to flex in both the vertical and horizontal directions but has the additional advantage of positioning pads 19 and 21 in vertical alignment with one another. As was described with respect to Figures 1 and 3, additional V-shaped holes 11 may be formed between the vias, as taught in Figure 2.

Figure 5 shows interposer 1 attached to chip die 23 by solder connections 25. The attachment of interposer 1, as shown in Figure 1, to chip die 23 is achieved by positioning interposer pads 7 against conventional corresponding high melt (250 - 360°C) C-4 solder bumps, previously attached to BLM pads 27 on chip die 23 in conventional manner. Upon heating, the high melt C-4 solder bumps collapse and solder is drawn through the respective copper plated vias 5 to copper pads 9 on the bottom surface of the interposer to form solder connectors. A solder stop layer may be temporarily positioned on the bottom surface of the interposer to limit the solder flow to the surface of pads 9. Thereafter the layer can be removed to expose pads 9. Alternatively, solder flow may be allowed to flow past the surface of pads 9 and, upon cooling, excess solder is trimmed flush with the surface pads.

Positioning interposer 1 in Figure 5 against the high melt C-4 solder bumps on chip die 23 and heating the solder so that it is drawn through vias 5

acts to simply and effectively provide a means of electrically connecting chip die metallurgy to conductive pads 9 on the bottom surface of interposer 1, and this is achieved without damaging the underlying circuitry on the chip die. After cooling, conventional low melt (170 - 200°C) solder balls 29 are attached to pads 9.

Figure 6 shows another arrangement for attaching interposer 1 to chip die 23. In this arrangement, flexible dielectric layer 3 described in Figure 1 is first laminated to the bottom of chip die 23 before any vias are formed. This may be done by placing the interposer and chip die in a lamination press and subjecting same, depending on materials, to heat (about 180 - 400°C) and pressure (about 250-2000 psi) for at least 1 hour. Then, the interposer material is laser ablated to form vias through to the underside of chip die 23 to expose BLM pads 27. The assembly is then cleaned to remove any contamination on surfaces inside the holes and on the interposer surface and these surfaces are then subjected to electroless copper plating. It can be seen that here, copper deposits not only on via walls at 15 but also at the bottom of the vias at 16 on BLM pads 27. Unwanted copper is then removed using the process described with respect to Figure 5, leaving copper at the bottom and side walls of the holes and at the interposer surface to form pads 9 around the holes. Thereafter, similar to Figure 5, low melt solder balls 29 are attached to pads 9 on the bottom of interposer 1.

Figure 7 shows a further arrangement for attaching interposer 1 to chip die 23. In this arrangement, a small amount of high melt solder is first deposited upon BLM pads 27 of chip die 23. Then, the interposer with the copper plated vias, as fabricated in accordance with the steps described with

regard to Figure 1, is positioned so that the interposer copper pads 7 align in contact with the solder deposits upon BLM pads 27. Next, the lamination steps described with regard to Figure 6 are employed to laminate the interposer 1 to chip die 23 whereby the high melt solder is drawn into the copper plated vias, similar to that described with respect to Figure 5 whereby a solder connection is made between chip die and interposer in a laminated configuration.

It can be seen that in Figures 6 and 7, interposer 1 is uniformly laminated against the surface of chip die 23. This is a result of the fact that the interposer material is sufficiently soft and resilient that it conforms to the small surface protrusions of the chip die and interposer pads at the chip die-laminate interface. In this regard, typical pad configurations only extend from .0001 to .0003 inches above the surface upon which they are deposited. However, it should be understood that although the surfaces of the chip die and interposer are bonded to one another, the interposer material is sufficiently elastic to provide the overall stress relief required for the chip die and electrical interconnections to maintain their integrity notwithstanding the differences in CTE between chip die 23 and circuit card 33.

Figure 8 shows the manner in which the arrangement of Figure 5 is attached to a circuit card. Low melt eutectic solder balls 29 in Figure 5 are first aligned in contact with chip pads 31 on circuit card 33. Upon heating, the solder balls melt and after cooling become soldered to pads 31. The same process is used in Figures 9 and 10 to attach the interposer/chip die structure of Figures 6 and 7 to circuit card 33.

A significant advantage is achieved in using low melt solder balls to attach the chip die/interposer package to circuit card 33. In this regard, use of the low melt solder allows the chip die/interposer package to easily be removed from circuit card 33 in the event rework is required, and this is done without destroying the chip die/interposer package.

It should be understood that any of the interposer configurations shown in Figures 1, 3 and 4, with or without the holes shown in Figure 2, may be used in the arrangements of Figures 5 through 10.

It should also be understood that although the arrangement in Figure 5 uses solder to connect to the chip die, it is possible to use plated dendrites on an electrically conductive adhesive bumped chip. Dendrites offer a non-solder solution which may be less susceptible to fatigue.

It will be understood from the foregoing description that various modifications and changes may be made in the preferred embodiment of the present invention without departing from its true spirit. It is intended that this description is for purposes of illustration only and should not be construed in a limiting sense. The scope of this invention should be limited only by the language of the following claims.

What is claimed is:

Claim(s)

1. An interposer for connecting a chip die directly to a circuit card comprising a layer of elastic dielectric material having an array of metal plated vias extending from one surface to the other each terminating in a metal pad with said vias sloped with respect to said surfaces.

2. The interposer as set forth in Claim 1 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

3. The interposer as set forth in Claim 2 wherein said elastic dielectric material has an array of holes therethrough positioned between said array of copper plated vias.

4. The interposer as set forth in Claim 3 wherein said elastic dielectric material is 10 to 15 mils thick and has an elastic modulus in the range of 50,000 to 400,000 psi.

5. An electronic package comprising:

a semiconductor chip die having an array of conductive pads on one surface thereof;

a flexible layer of dielectric material having an array of metal plated vias extending therethrough to opposing surfaces thereof with said array

corresponding to said array of conductive pads on said chip die and with each of said vias terminating in a metal pad on each of said opposing surfaces with each said metal pad on one of said surfaces connected by solder to respective ones of said array of conductive pads on said chip die; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said surfaces of said flexible layer and connected by solder thereto.

6. The electronic package of Claim 5 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

7. The electronic package of Claim 5 wherein said copper plated vias of said flexible layer are formed by two segments each sloped with respect to an opposing surface and meeting internal to said surfaces to form a V-shaped copper plated via.

8. The electronic package of Claim 5 wherein the said copper plated vias of said flexible layer are sloped with respect to said opposing surfaces of said layer.

9. The electronic package of Claim 5 wherein said flexible layer has an array of holes therethrough positioned between said array of copper plated vias.

10. The electronic package of Claim 5 wherein said copper pads on said one of said surfaces is connected to said array of conductive pads on said chip die by a copper plated connection.

11. The electronic package of Claim 5 wherein said flexible layer is a low elastic modulus material.

12. The electronic package of Claim 5 wherein said flexible layer has an elastic modulus in the range of 50,000 to 400,000 psi.

13. The electronic package of Claim 5 wherein said copper plated vias are filled with solder.

14. A method of connecting a semiconductor chip die having an array of conductive pads on one surface thereof to a circuit card having a corresponding array of conductive pads, comprising the steps of:

forming a flexible interposer to electrically connect said chip die to a circuit card by forming an array of metal plated vias in a layer of flexible material positioned to correspond to said array of conductive pads on said chip die with each via terminating on opposing surfaces of said layer of flexible material in metal connection pads;

attaching first solder bumps to each pad of said array of conductive pads on said one surface of said chip die;

positioning said flexible interposer so as to align and contact said array of metal pads on one surface of said flexible material with said first solder bumps attached to said conductive pads on said chip die;

heating said first solder bumps to melt and draw said solder into each of said metal plated vias to fill said vias to said metal pads on the other surface of said flexible material and electrically attach said array of metal pads on said one surface to said array of conductive pads on said chip die;

attaching second solder bumps to each pad of said metal pads on said other surface of said flexible material;

positioning the said array of conductive pads on said circuit card so as to align and contact said second solder bumps attached to said metal pads on said other surface of said flexible material; and

applying heat to said second solder bumps attached to the said metal pads on said other surface of said flexible material so as to melt said second solder bumps to electrically attach said array of metal pads on said other surface to said array of conductive pads on said circuit card.

15. The method as set forth in Claim 14 wherein said first solder bumps comprise a high melt solder.

16. The method as set forth in Claim 15 wherein said second solder bumps comprise a lower melt solder than said high melt solder.

17. The method as set forth in Claim 16 wherein said array of metal plated vias each terminating in a metal pad is an array of copper plated vias each terminating in a copper pad.

18. The method as set forth in Claim 17 wherein said layer of flexible material has an elastic modulus between about 50,000 to 400,000 psi.

19. The method as set forth in Claim 18 wherein said vias are sloped with respect to the surfaces of said layer of flexible material.

20. The method as set forth in Claim 14 wherein the step of forming a flexible interposer includes the additional step of forming an array of holes positioned between said array of copper plated vias.

21. A method of connecting a semiconductor chip die having an array of conductive pads on one surface thereof to a circuit card having a corresponding array of conductive pads, comprising the steps of:

laminating one surface of a layer of flexible dielectric material to said chip die;

forming an array of holes through said layer of flexible material at locations to expose said conductive pads on said chip die;

depositing metal in said array of holes to provide a conductive connection from said conductive pads on said chip die to conductive pads formed thereby on the other surface of said flexible material;

attaching solder bumps to said conductive pads on said other surface of said flexible material;

positioning said array of conductive pads on said circuit card so as to align and contact said solder bumps attached to said conductive pads on said other surface of said flexible material; and

applying heat to said solder bumps to electrically attach said array of conductive pads on said circuit card to said conductive pads on said other surface of said flexible material.

22. The method as set forth in Claim 21 wherein said lamination step comprises laminating in a lamination press at between 180 and 400°C and 250 and 2000 psi for at least 1 hour.

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Abstract of the Disclosure

A flexible, compliant layer of a single low modulus material for connecting a chip die directly to a circuit card without encapsulation. The flexible compliant layer provides stress relief caused by CTE thermal mismatch in chip die and circuit card. An array of copper plated vias are formed in said compliant layer with each via terminating on opposing surfaces of the layer in copper pads. Rather than copper, other metals, such as gold or nickel, may also be used. An array of holes may be positioned between said array of vias to provide additional resiliency. The plated vias may be angled with respect to said opposing surfaces to allow additional vertical and horizontal stress relief. Connection of the pads on one surface to high melt C-4 solder balls or columns on a chip die results in solder filled vias. Low melt solder connection of the pads on the other surface to a circuit card allows non-destructive rework of the cards.

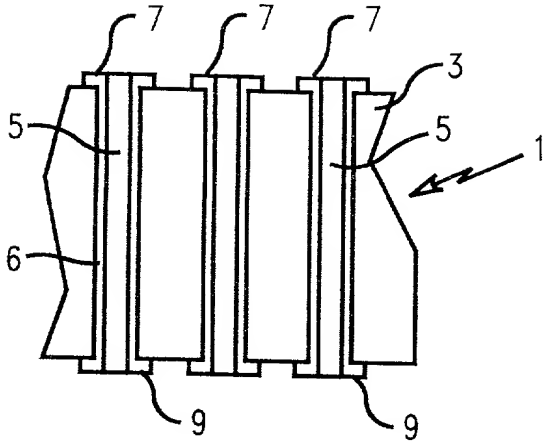

FIG. 1

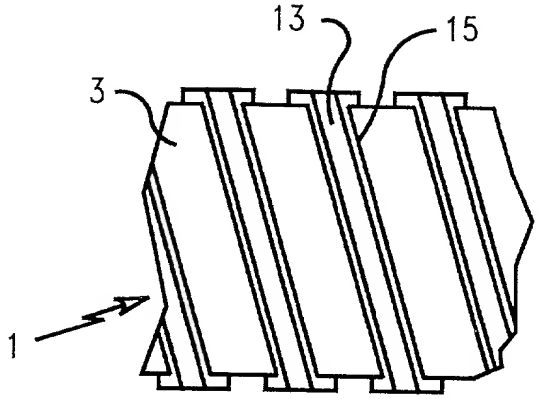

FIG. 3

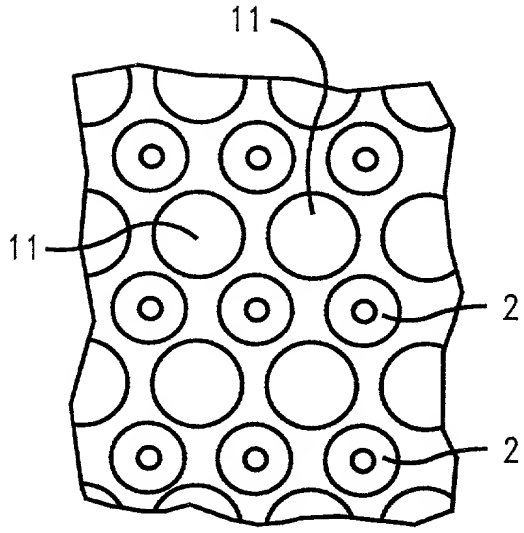

FIG. 2

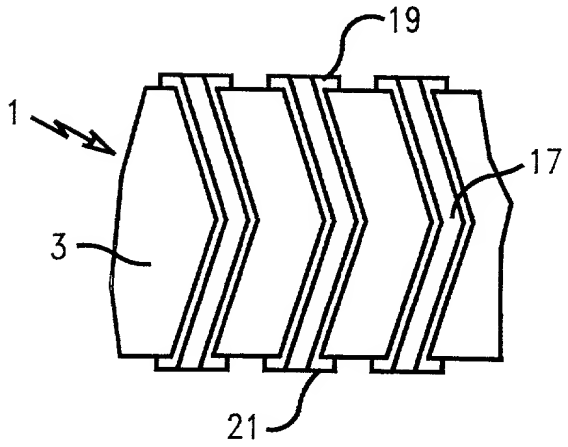

FIG. 4

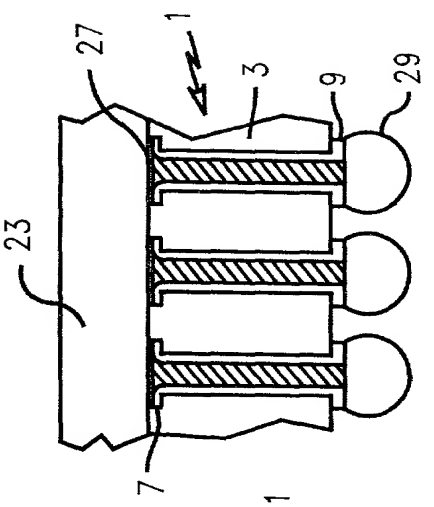

FIG. 7

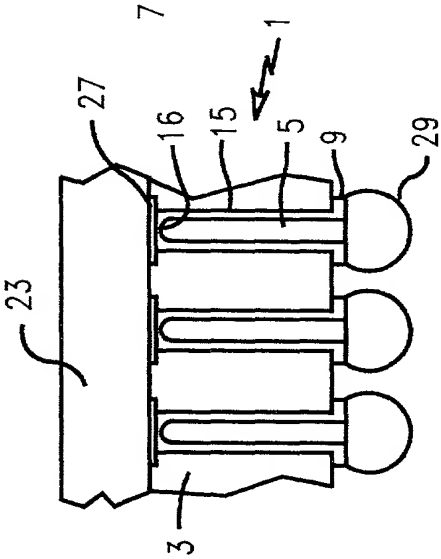

FIG. 6

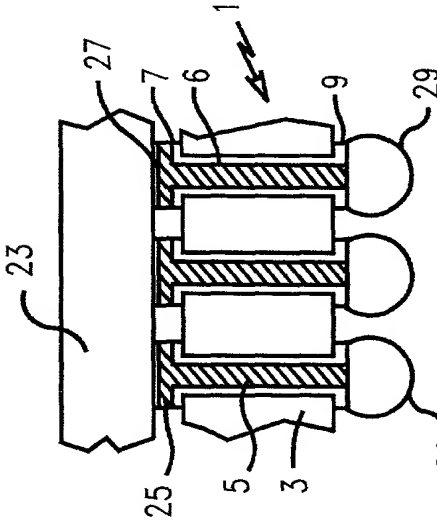

FIG. 5

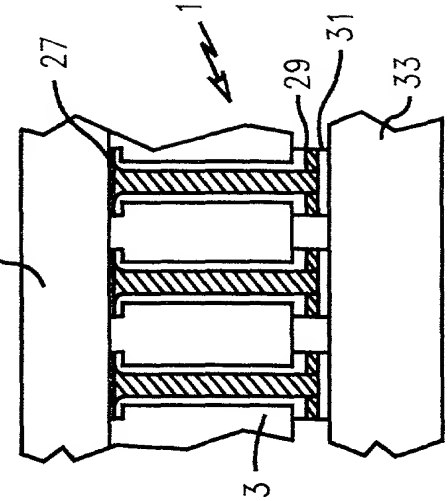

FIG. 10

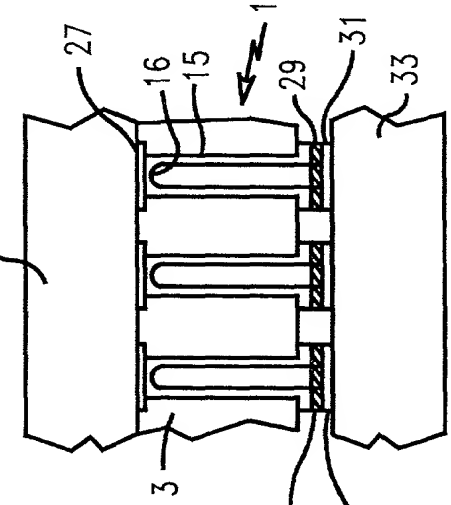

FIG. 9

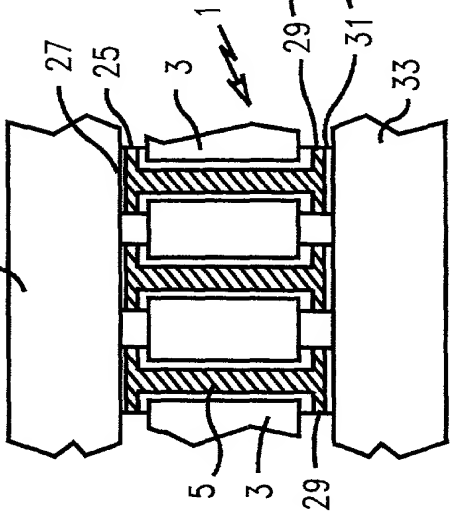

FIG. 8

Declaration and Power of Attorney for Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

FLOATING INTERPOSER

the specification of which (check one)

[x] is attached hereto.

[ ] was filed on _____ as Application Serial No. _____ and was amended on _____ ____.

I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year Priority Claimed
N/A		

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status
N/A		

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: David L. Adour, Registration No.

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